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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of listings of claims in the application.

- 1 1. (previously presented) A semiconductor device having at least one transistor, the
- 2 device comprising:
- 3 a substrate having a channel region defined thereon;
- 4 a first insulating layer disposed over said channel region and over at least a
- 5 portion of said substrate;
- 6 a floating gate having at least a substantial portion thereof disposed over said
- 7 channel region and separated therefrom by said first insulating layer, said floating
- 8 gate having at least two side walls and a top surface;
- 9 a second insulating layer disposed over said side walls and over said top surface
- 10 of said floating gate;
- 11 a control gate having a first portion disposed over a portion of said channel region
- 12 and being separated therefrom by said second insulating layer, a second portion
- 13 formed over a first one of said side walls and a third portion formed over at least a
- 14 first portion of said top surface of said floating gate and being separated from said
- 15 floating gate by said second insulating layer, said second portion having a surface
- 16 substantially parallel to and opposing said first side wall;
- 17 an erase gate formed over a second one of said side walls and over at least a
- 18 second portion of said top surface of said floating gate and being separated from
- 19 said second one of said side walls and said portion of said top surface of said
- 20 floating gate by said second insulating layer;
- 21 a drain region formed in a portion of said substrate proximate said first portion of
- 22 the control gate; and
- 23 a source region formed in a portion of said substrate proximate said erase gate,
- 24 said source region having a substantial portion thereof underneath said floating

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- 25 gate;
26 wherein during an erase operation with the drain region, the source region and the
27 control gate connected to ground, and a relatively high potential applied to the
28 erase gate, stored electrons are removed from the floating gate to the erase gate
29 through the Fowler-Nordheim tunneling process.
- 1 2. (Previously presented) A semiconductor device having at least one transistor as
2 recited in claim 1, wherein said erase gate overlaps said floating gate and at least a
3 portion of said control gate.
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
- 1 8. (Previously presented) A memory array disposed on a substrate comprising a
2 plurality of memory cells each having a channel region formed in said substrate, a
3 floating gate separated from said channel region by a first insulating layer, an
4 erase gate, a control gate separated from said floating gate by a second insulating
5 layer, a source region, and a drain region, comprising:
6 a plurality of rows and columns of interconnected memory cells wherein the
7 control gates of memory cells in the same row are connected by a common word-
8 line, the erase gates of the memory cells in the same row are connected by a
9 common erase line, the source regions of the memory cells in the same rows are
10 connected by a common source line, and the drain regions of memory cells in the

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11 same columns are commonly connected via a common drain line, wherein at least
12 a portion of each said control gate is disposed over a portion of said channel
13 region and is separated therefrom by said second insulating layer, said portion of
14 the control gate being proximate to said drain region, and wherein a portion of
15 said control gate is disposed in facing relationship to a side surface of said
16 floating gate and is separated therefrom by said second insulating layer; and
17 a control circuit connecting to said word-lines, erase lines, source lines and drain
18 lines for operating one or more memory cells of said memory array;
19 wherein said source region having a substantial portion thereof underneath said
20 floating gate, and wherein during an erase operation with the drain region, the
21 source region and the control gate connected to ground, and a relatively high
22 potential applied to the erase gate, stored electrons are removed from the floating
23 gate to the erase gate through the Fowler-Nordheim tunneling process.

1 9. (Previously presented) A memory array disposed on a substrate as recited in claim
2 8 wherein said floating gate has a least a substantial portion thereof disposed over
3 said channel region and is separated therefrom by said first insulating layer, said
4 control gate is substantially placed on one side of said floating gate and separated
5 therefrom by said second insulation layer, said erase gate is substantially placed
6 on a second side of said floating gate and is separated therefrom by said second
7 insulation layer, said drain region is substantially disposed on said on side of said
8 floating gate, and said source region is substantially disposed on said second side
9 of said floating gate.

10. (Previously presented) A memory array as recited in claim 9, wherein said erase
gate overlaps said floating gate and at least a portion of said control gate.

11. (Cancelled)

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12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled).

24. (Cancelled).

25. (Cancelled)